

# Development of the Continuous Acquisition Pixel (CAP) sensor for high luminosity lepton colliders

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## Abstract

A future higher luminosity B-factory detector and concept study detectors for the proposed International Linear Collider require precision vertex reconstruction while coping with high track densities and radiation exposures. Compared with current silicon strip and hybrid pixels, a significant reduction in the overall detector material thickness is needed to achieve the desired vertex resolution. Considerable progress in the development of thin CMOS-based Monolithic Active Pixel Sensors (MAPS) in recent years makes them a viable technology option and feasibility studies are being actively pursued. The most serious concerns are their radiation hardness and their readout speed. To address these, several prototypes denoted as the Continuous Acquisition Pixel (CAP) sensors have been developed and tested. The latest of the CAP sensor prototypes is CAP3, designed in the TSMC 0.25  $\mu\text{m}$  process with a 5-deep Correlated Double Sample (CDS) pair pipeline in each pixel. A setup with several CAP3 sensors is under evaluation to assess the performance of a full-scale pixel readout system running at realistic readout speed. Given the similarity in the occupancy numbers and hit throughput requirements, per unit area, between a Belle vertex detector upgradation and the requirements for a future ILC pixel detector, this effort can be considered a small-scale functioning prototype for such a future system. The results and plans for the next stages of R&D towards a full Belle Pixel Vertex Detector (PVD) are presented.

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## 1. Introduction

It has long been known that the vertexing performance of a silicon tracker could be improved by incorporating a fine granularity pixel detector in its innermost layer. Hybrid pixel detectors are the baseline for the experiments

[1–3] under construction at the LHC collider at CERN. Their technology is well established and they provide a detector with high rate handling capability and pixel level hit treatment. In the case of a B-factory, where the tracks have relatively low momenta and the resolution is limited by multiple scattering, preliminary studies [4] indicated that the most important aspects to improve the resolution are moving the vertex detector as close to the interaction point (IP) as possible and reducing the amount of material in

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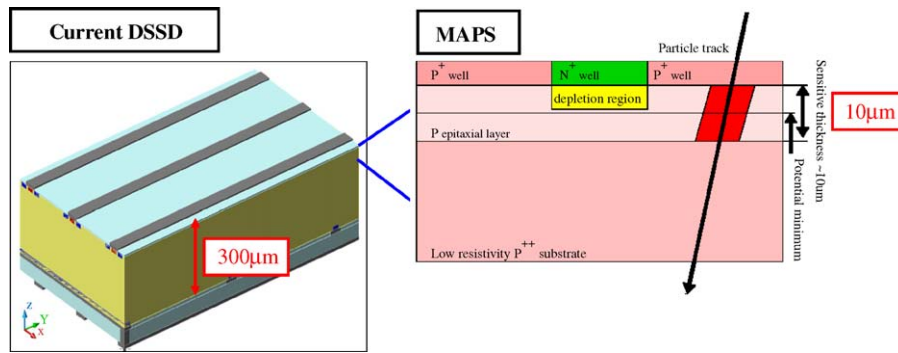


Fig. 1. A comparison of standard Double Sided Strip Detectors (DSSDs) with MAPS devices. The pF capacitances typical of long DSSDs can be reduced to fF in the MAPS case, drastically reducing the required thickness of detector needed for detecting a minimum ionizing particle passage with high SNR.

each detector layer. The rather thick hybrid pixel detectors ( $\sim 750\ \mu\text{m}$  of silicon,  $\sim 0.8\%$  rad. length for each pixel layer) are thus not suitable. Similar constraints on multiple-scattering also drive an ILC vertex detector away from a hybrid pixel solution. For the observation of time-dependent CP violation in the gold-plated  $B \rightarrow J/\psi K_S$  mode with Belle [5], the  $\sim 100\ \mu\text{m}$  vertexing resolution based on the Silicon strip Vertex Detector (SVD) [6] measurements was sufficient and the development of a B-factory specific pixel detector has not been aggressively pursued. As KEKB [7] has become the highest luminosity collider in the world, operating with sustained luminosities exceeding  $10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}$ , radiation damage and high occupancy of the SVD have become major issues. New vertexing solutions are needed for the proposed super B-factory upgradation [8], where the background is expected to increase 20–50 times. Also, to fully exploit the physics reach, as many interesting decay modes are background limited, better vertexing resolution is desired to suppress these backgrounds.

Recent advances in the development of the CMOS based deep submicron Monolithic Active Pixel Sensors (MAPS) make them a promising candidate for the upgradation. The charge in a MAPS device is collected by thermal diffusion in about  $10\ \mu\text{m}$  thick epitaxial layer of the chip without any bias voltage applied. This is contrasted in Fig. 1 with the situation for the standard Double Sided Strip Detector (DSSD) employed in the current Belle SVD. Because the DSSD strip capacitance is large, of the pF order, a thick detector is necessary to ensure sufficient signal-to-noise ratio (SNR). In contrast, since the MAPS pixel capacitance can be made in the fF capacitance range, the devices can be made with a thin detection volume. Indeed, since the rest of the silicon substrate is largely only there for mechanical reasons, these devices can be thinned and will much better match the relatively low momentum particle environment of a B-factory operating at the  $\Upsilon(4S)$  resonance. The basic functionality of the MAPS technology has already been established for high precision tracking [9], though as of yet no experiment has operated a detector based upon this technology. Indeed, four key aspects remain to be proven

before they can be accepted for use in Super Belle detector. These are

- (1) the readout speed,
- (2) radiation hardness,
- (3) operation experience with full-sized detectors,
- (4) fabrication and handling of thinned detectors.

An active program has been undertaken to address these issues and a status report is provided in this paper.

## 2. The CAP architecture

The choice of the sensor architecture depended heavily on the specific requirements posed by the Belle detector and the KEKB collider environment. In KEKB, with total stored currents exceeding 1 A for electrons and 2 A for positrons and the bunches colliding with as little as 2 ns separation, the beam is essentially DC in terms of timing structure as observed in the detector. However, with such large stored energy it is necessary to provide a beam abort gap to safely dump the beam when a machine element fails, beam conditions deteriorate, or one of the frequent earthquakes occurs. The beam timing structure can be seen in the top part of Fig. 2. As discussed below, this bunch structure is exploited to provide deadtimeless pixel operation. It should be noted that these large currents induce accumulated doses in excess of  $2\ \text{kGy}\ \text{yr}^{-1}$  in the innermost layer of the present SVD2, where the occupancy is now 10%. To be able to operate in the future Super-KEKB environment, a variant of the standard MAPS, denoted the Continuous Acquisition Pixel (CAP) was designed. The design concept of a CAP sensor is simple: a standard MAPS 3-transistor cell, consisting of a reset, sense and select transistor is used, surrounded by an infrastructure that enables it to be read out as fast as possible. Electrons from deposited ionization are collected on the gate of the sense transistor, which has to be periodically reset to restore the collection potential. Data is extracted using the Correlated Double Sampling (CDS) method, which means a subtraction of two frames of the

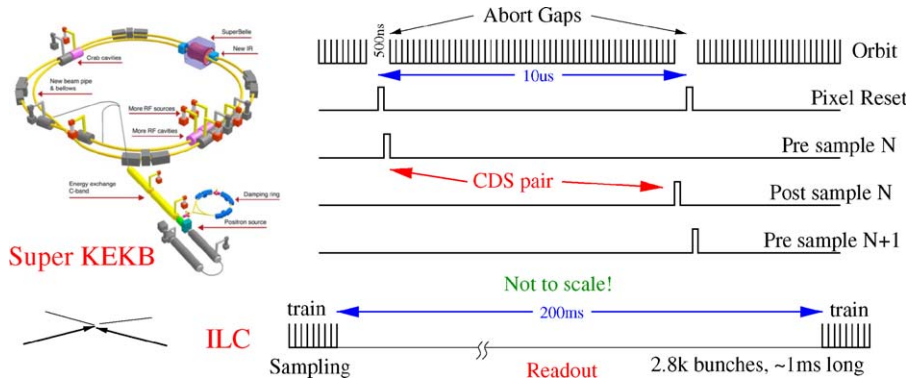


Fig. 2. Machine bunch structure and correlated double sampling timing structure for the Super Belle and ILC pixel detectors.

potential level of the sense transistors with a certain integration time between the frames. This subtraction removes the contributions of the fluctuations due to the reset procedure.

### 2.1. CAP1 and CAP2 results

To investigate the basic properties of MAPS detectors and their suitability for a Belle pixel upgrade, two small-scale prototypes were fabricated. Both were  $132 \times 48$  arrays, implemented in the TSMC<sup>1</sup> 0.35  $\mu\text{m}$  process. The pixel size was chosen to be  $22.5 \mu\text{m} \times 22.5 \mu\text{m}$  as an optimum between the number of readout pixels and the single point resolution. The 48 common row output bus lines are multiplexed by  $4 \times 12$  parallel analog output streams. The difference between the CAP1 and CAP2 designs is, although the physical dimensions and the pixel size are the same, that the latter includes a miniature 8-deep pipeline in each pixel. The pipeline makes it possible to decouple the frame sampling rate from the triggered readout rate and thus to reduce the data transfer rate from the chip by the ratio of the sampling to the trigger rates. In the case of the  $10 \mu\text{s}$  integration time required for occupancy reasons and  $10 \text{ kHz}$  trigger rate expected at Super Belle, this buffering gains about an order of magnitude reduction in the data transfer size. In addition to verifying the MAPS performance as reported in the literature, a study of possible degradation of SNR at high framing rates and a study of radiation damage was performed. An array of four CAP1 detectors was tested in a  $4 \text{ GeV}$  pion beam at the KEK Proton Synchrotron beam test facility in 2004. Clear hit coincidences in all four layers were observed. The beam test yielded intrinsic resolution of  $11 \mu\text{m}$  dominated by the multiple scattering, and an SNR of  $\sim 20$ . Further, a number of CAP1 sensors were irradiated to 2, 30 and  $200 \text{ kGy}$  using a  $^{60}\text{Co}$  gamma source and the threshold voltage shift in the  $0.35 \mu\text{m}$  TSMC process was found to be acceptable. The leakage currents after irradiation and annealing are comparable to previous results [10]. After  $200 \text{ kGy}$  CAP1 retained full functionality

and the effects at higher doses are not yet explored due to the time constraints of the irradiation facility. The results of CAP1 beam-test and radiation damage studies are presented in detail elsewhere [11,12].

### 2.2. The CAP3 design and plans for a Pixel Vertex Detector

Based on the successful operation of CAP1 and CAP2 prototypes, effort was directed towards fabricating a full-size Pixel Vertex Detector (PVD). Thus the third generation prototypes (CAP3), designed in the TSMC  $0.25 \mu\text{m}$  process, were fabricated. The fabrication cost of the chip increases considerably at larger die sizes and is limited to about  $21 \text{ mm}$  in one direction by the maximum standard reticle size. Considering these constraints, a  $3 \text{ mm} \times 21 \text{ mm}$  CAP3 prototype was designed consisting of a  $928 \times 128$  pixel array at  $22.5 \mu\text{m}$  pitch, with a 5-deep sample pair pipeline in each pixel. While these could be treated as 10 independent samples, it is planned to use them, for operational convenience, as five CDS signals for direct use as differential reads. The  $\sim 120 \times 10^3$  pixels of a single CAP3 chip (Fig. 3) correspond roughly to the number of the readout channels of the present entire DSSD based SVD2. As stated in item (1) of the R&D issues, making a readout system capable of handling the enormous amount of data intrinsic to such a finely segmented detector is crucial.

As with the CAP2 prototype, the decoupling of the sampling frequency from the readout frequency makes it possible to reduce the required data flow from CAP3, which would nevertheless at  $10 \text{ kHz}$  trigger rate still correspond to about  $1.2 \times 10^9$  sample pairs  $\text{s}^{-1}$ . Data are transferred via 32 signal channels, with transfer rates of about  $100 \text{ MHz}$  to meet the latency requirements.

The task of the CAP3 front-end readout system (PIXRO) is to differentiate the analog CDS pairs on the fly and transmit these reduced signals via optical fiber link to the back-end electronics. The current baseline design is a high speed analog multiplexer, with the data digitalization on the back-end (COPPER/FINESSE) side [13] of the optical link. The PIXRO1 chip is implemented in the IBM  $0.5 \mu\text{m}$  SiGe BiCMOS 5HP

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Fig. 3. Overview photo of a CAP3 test setup, with zoomed die views inset. The CAP3 die is reticle-size limited at about 21 mm in length and consists of 926 columns  $\times$  128 rows of pixels, corresponding to just under 120 k pixels. Reading out at 10 kHz of triggered frame rates requires a throughput of over 1 Giga CDS pairs  $s^{-1}$ .

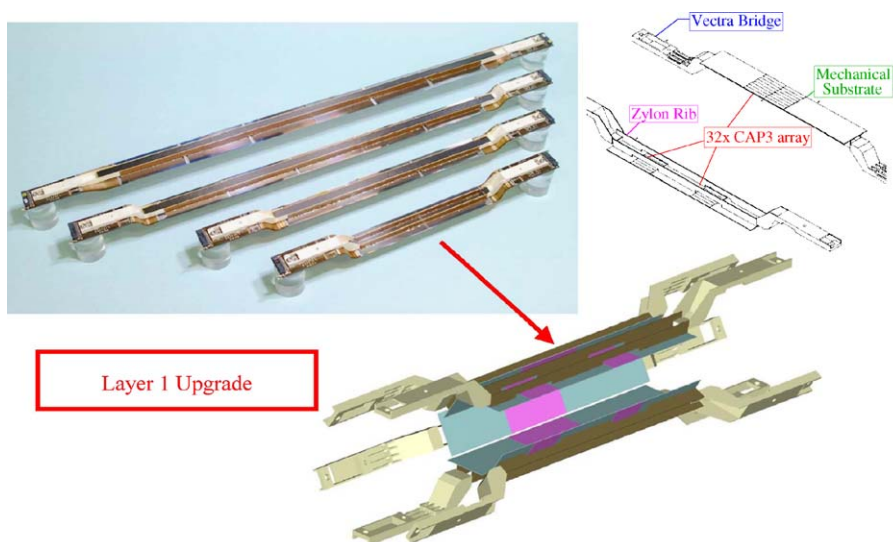


Fig. 4. An option for a short-term upgrade to the Belle silicon tracking system. In this case, the innermost layer is replaced with an array of CAP3 detectors. Mechanically these are drop-in replacements for the current Layer 1 DSSD ladders. As seen, there are six Layer 1 ladders, each of which hold an array of  $4 \times 8$  CAP3 in  $z$  and  $r - \phi$ , respectively, corresponding to just over 23 million pixels.

process<sup>2</sup> and can readout and differentiate two full CAP3 frames in up to 100  $\mu s$ , which satisfies the Super Belle requirements.

### 2.3. Short-term upgrade path

An ultimate vertex detector geometry for the pixel detector would involve reducing the beam pipe radius and thus requires a significant redesign of the accelerator and interaction region. An immediate upgradation to address the issue of occupancy is well underway [14]. Neither this

upgradation nor a proposed short-strip (“striplet”) upgradation [14] will improve the vertex resolution, though they will improve the occupancy robustness. Therefore, in short term an option to improve the vertexing is to replace the innermost ladder array with an array of CAP3 detectors. Mechanical design studies have begun, as may be seen in Fig. 4. In this configuration, the pixel layer will consist of about 23 M pixels.

## 3. ILC prototype

For both Super B factory and the ILC [15], readout is optimized for the machine bunch structure, as indicated in Fig. 2. Despite the difference in center of mass energy, the

<sup>2</sup>By MOSIS Integrated Circuit Fabrication Service, USC Information Sciences Institute, Marina del Rey, USA.

Table 1  
Comparison of Super B-factory and ILC vertex operating conditions

Parameter	ILC	Super-B	Notes
Integration time	25 $\mu\text{s ms}^{-1}$	$\leq 10 \mu\text{s}$	Belle (trigger dep.)
BX collision timing	300 (150) ns	2 ns	
# bunches/integ. time	75(150)/2.8 k	1–5 k	CPCCD or MAPS/DEPFET for ILC
Expected occupancy	$\sim 1\%$	$\sim 0.5\text{--}1\%$	Belle extrapolation
# pixel channels (million)	100s to 1000s	10–50	five layers versus single
Duty cycle (high power)	few %	5–10%	within acceptance
Readout cycle	between trains	continuous	
Pixel readout rate (raw)	500/10 Gpix $\text{s}^{-1}$	200–1000 Gpix $\text{s}^{-1}$	Belle 10 kHz trigger
Radiation requirements	0.5 kGy $\text{yr}^{-1}$	few 10 kGy $\text{yr}^{-1}$	NIEL not considered

requirements on occupancy and low-power operation are not so different. These parameters are compared in Table 1, where for the ILC case often two numbers are listed. The first refers to detector technologies such as CAPS, which sample multiple times within a bunch train; whereas the second number refers to detector technologies such as DEPFETs, which integrate for the full bunch train.

### 3.1. Pixel packing density

An obvious question that arises as part of addressing the issue of providing in-pixel storage is the maximum depth. Reducing the storage cell size obviously extends the number of possible sample buffers. However, with the very small capacitances involved, the process of storing itself adds a “ $kTC$ ” noise term:

$$v_{\text{noise}} = \sqrt{\frac{kT}{C}}. \quad (1)$$

In the  $0.25 \mu\text{m}$  process being considered, this contribution is not negligible. For instance, as reported above, the typical noise seen in CAP1 was  $16 e^-$ , whereas for CAP2 it was  $\sim 30 e^-$ . With very small charges to begin with, typically a few hundred  $e^-$  in the peak pixel, this can obviously lead to a degradation of  $SNR$ . Currently the CAP3 has 10 storage cells and given that they have similar capacitance to CAP2, it is expected that the contributed noise should be comparable. In terms of going to a deeper submicron fabrication process, it should be possible to pack in more storage cells. However, as the storage capacitance decreases, the effect can become dramatic. For the case of a  $3.2 \text{ fF}$  collection electrode

$$\Delta V = \frac{\Delta Q}{C} = \frac{1.6 \times 10^{-19} \text{ C}}{3.2 \times 10^{-15} \text{ F}} = 50 \mu\text{V}/e^- \quad (2)$$

the corresponding contribution due to the sample storage is seen as in Fig. 5.

Therefore a direction for future exploration, where a deeper sampling pipeline is needed in such a small cell, will be to investigate means to increase the capacitance of the basic storage cell.

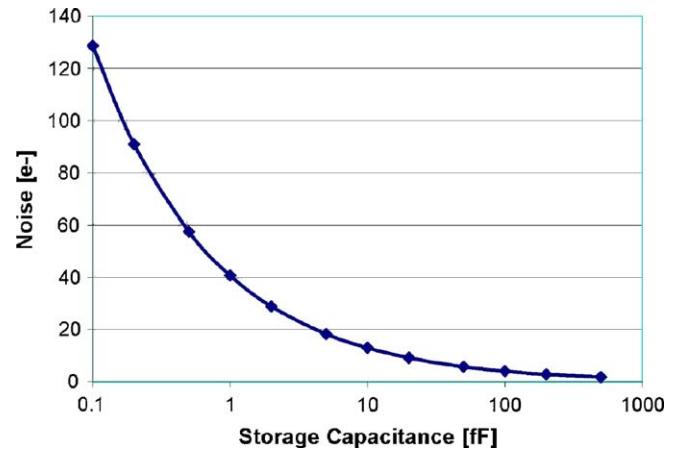


Fig. 5. Contribution to noise due to storage cell capacitance. For small storage cells, this term can become dominant and make the  $SNR$  unacceptably low.

### 3.2. Low duty cycle operation

Another crucial issue with ultra-thin detectors is the ability to extract self-heat from these active detector devices. Addition of material to provide cooling would defeat the gains provided by such thin devices. One tool in addressing the issue is to power off high power consuming elements of the detector whenever possible. Indeed, this is the baseline being considered as noted in Table 1. However, it remains to be demonstrated that the circuitry and biases can be run in this mode without deleterious impact on performance. This item is under study with CAP3 and will be reported on later.

## 4. Conclusions and future plans

After encouraging preliminary results of radiation hardness studies performed with CAP1 prototypes and the study of pipelined readout with CAP2 prototypes, CAP design looks promising for application in Belle. The physical dimensions of the CAP3 chip are large enough to be able to use it directly as a building block of the first generation pixel detector. In the initial PVD upgradation, the plan is to keep the mechanical structure of the present

Belle SVD2 system [14], which permits the possibility of an earlier installation without a redesign of the interaction region. CAP sensors would be used instead of the DSSD in the first layer of the SVD only. The mechanical support for the first layer DSSD has the form of six independent slightly overlapping planes (ladders), and each of these ladders can be fully populated using 36 CAP3 sensors per ladder. The operation of CAP3 sensor together with its readout system is being extensively tested in the laboratory environment and a beam-test experiment is in preparation.

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