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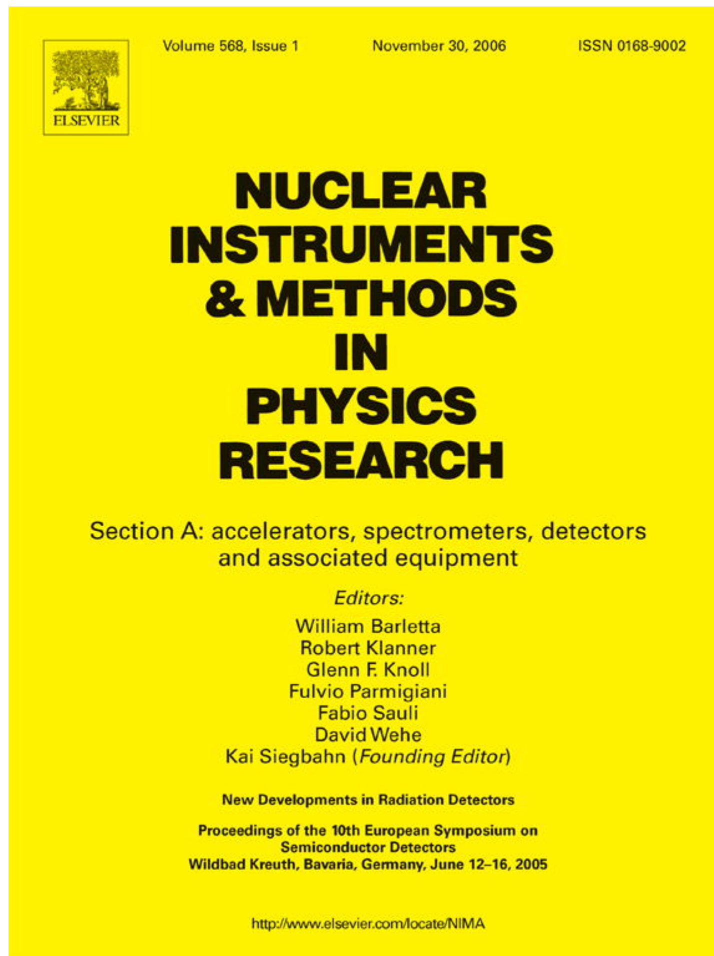

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Recent progress in the development of a B-factory monolithic active pixel detector

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Abstract

Due to the need for precise vertexing at future higher luminosity B-factories with the expectedly increasing track densities and radiation exposures, upgrade of present silicon strip detectors with thin, radiation resistant pixel detectors is highly desired. Considerable progress in the technological development of thin CMOS based Monolithic Active Pixel Sensors (MAPS) in the last years makes them a realistic upgrade option and the feasibility studies of their application in Belle are actively pursued. The most serious concerns are their radiation hardness and their read-out speed. To address them, several prototypes denoted as Continuous Acquisition Pixel (CAP) sensors have been developed and tested. The latest of the CAP sensor prototypes is CAP3, designed in the TSMC 0.25 μm process with a 5-deep sample pair pipeline in each pixel. A setup with several CAP3 sensors will be used to assess the performance of a full scale pixel read-out system running at realistic read-out speed. The results and plans for the next stages of R&D towards a full Pixel Vertex Detector (PVD) are presented.
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1. Introduction

It has long been known that the vertexing performance of a silicon tracker could be improved by incorporating a pixel detector in its innermost layer. Hybrid pixel detectors are the baseline for the experiments [1,2] at the future LHC collider at CERN. Their technology is well established and they provide a detector with fine granularity and with information treatment at pixel level. In the case of a B-factory, where the tracks have relatively low momenta and the resolution is limited by multiple scattering, preliminary studies [3] indicated that the most important aspects to improve the resolution are moving the vertex detector as close to the interaction point (IP) as possible and reducing the amount of material in each detector layer. Rather thick hybrid pixel detectors (~750 μm of silicon, ~0.8% rad. length for each pixel layer) are thus not suitable. For the observation of CP violation in the gold-plated mode $J/\psi K_S$ with Belle [4], the vertexing resolution based on the silicon strip detector (SVD) [5] measurements was sufficient and the development of a B-factory specific pixel detector was not aggressively pursued at that time. As KEKB [6] has become the collider with the highest luminosity in the world, radiation damage and high occupancy of the SVD became major issues. New vertexing solutions are needed

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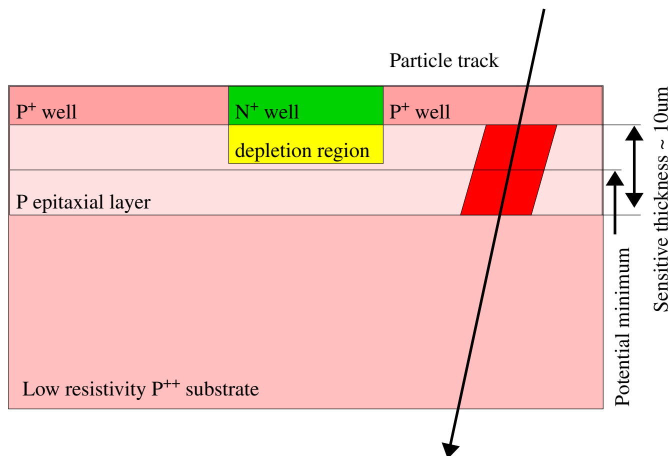

Fig. 1. Schematic view of an ionizing particle passing through a MAPS device.

for the proposed Super B-factory upgrade [7], where the background is expected to increase 20–50 times and better vertexing resolution is desired.

Recent advances in the development of the CMOS based deep sub-micron monolithic active pixel sensors (MAPS) make them a promising candidate for the upgrade. The charge in MAPS is collected by diffusion in the about 10 μm thick epitaxial layer of the chip without any bias voltage applied (Fig. 1). They can be thinned and will much better match the relatively low momentum particle environment of a B-factory operating at the $\Upsilon(4S)$ resonance. As the basic functionality of the MAPS technology has already been established for high precision tracking, four main aspects remain to be proven before they can be accepted for use in SuperBelle. These are the read-out speed, radiation hardness, operation experience of full-sized detectors and fabrication feasibility of thinned detectors, the first three of which will be covered in this report.

2. The CAP architecture

The choice of the sensor architecture depended heavily on the specific requirements posed by the Belle detector and the KEKB collider environment. In KEKB, with total stored currents exceeding 1A for electrons and 2A for positrons and the bunches colliding with as little as 2ns separation, the beam looks almost as DC current in terms of timing structure as observed in the detector. Large currents induce accumulated doses in excess of 2 kGy/year in the innermost layer of the present SVD2, where the occupancy is now 10%. To be able to operate in the future SuperKEKB environment, a variant of the standard MAPS, denoted the Continuous Acquisition Pixel (CAP) was designed. The design concept of a CAP sensor is simple: a standard MAPS 3-transistor cell, consisting of a reset, sense and select transistor is used, surrounded by an infrastructure that enables it to be read out as fast as possible. Electrons from deposited ionization are collected on the gate of the sense transistor, which has to be periodically reset to restore the potential. Data is extracted using the correlated double sampling (CDS) method, which means a subtraction of two frames of the potential level of the sense transistors with a certain integration time between the frames. This subtraction removes the contributions of the fluctuations due to the reset procedure.

2.1. The CAP1 and CAP2 design and operation

The CAP1 prototype is a 132×48 array of simple 3-transistor MAPS cells, implemented in the TSMC[1] 0.35 μm process. The pixel size was chosen to be $22.5 \times 22.5\,\mu m^2$ as an optimum between the number of read-out pixels and the single point resolution. The 48 common row output bus lines are multiplexed by 4 onto 12 parallel analog output streams. The conceptual difference between CAP1 and CAP2 design is, although the physical dimensions and the pixel size are the same, that the later includes a miniature 8 deep pipeline in each pixel. The pipeline makes it possible to decouple the frame sampling rate from the read-out rate and thus to reduce the data transfer rate from the chip by the ratio of the sampling to the trigger rate. In the case of 10 μs integration time required for occupancy reasons and 10 kHz trigger rate expected at SuperBelle, this concept gains about an order of magnitude reduction in the data transfer size. Both the CAP1 and CAP2 were read out using the same front-end and back-end board scheme. A front-end board (F2) contains the CAP chip itself, a 10-bit ADC converter and analog support electronics. The data is broadcast over a high speed LVDS serial link at approximately 400 Mb/s and is connected to the back-end (B2) board via standard Cat.5 Ethernet cables. Four F2 boards are read by a single B2 board to ease the event synchronization. Data from the B2 board is collected over a PCI interface by an embedded Linux based computer. The difference between CAP1 and CAP2 operation lies in the way the data flow is controlled by some programmable gate array chips on F2 and B2, as well as changes in the data acquisition software. Event acquisition for full frame pairs from four detectors including the 8 ms integration time was measured to be about 30 Hz. In addition to verifying the MAPS performance as reported in the literature, a study of possible degradation of signal-to-noise ratio (SNR) at high framing rates and a study of radiation damage was performed. An array of four CAP1 detectors was tested in a 4 GeV pion beam of the KEK beam test-facility in 2004. Clear hit coincidences in all four layers were observed. The beam-test yielded intrinsic resolution of 11 μm dominated by the multiple scattering, and signal vs. noise ratio of ~20. Further, a number of CAP1 sensors were irradiated to 2, 30 and 200 kGy using a ^{60}Co gamma source and the threshold voltage shift in the 0.35μm TSMC process was found to be acceptable. The leakage currents after irradiation and annealing are

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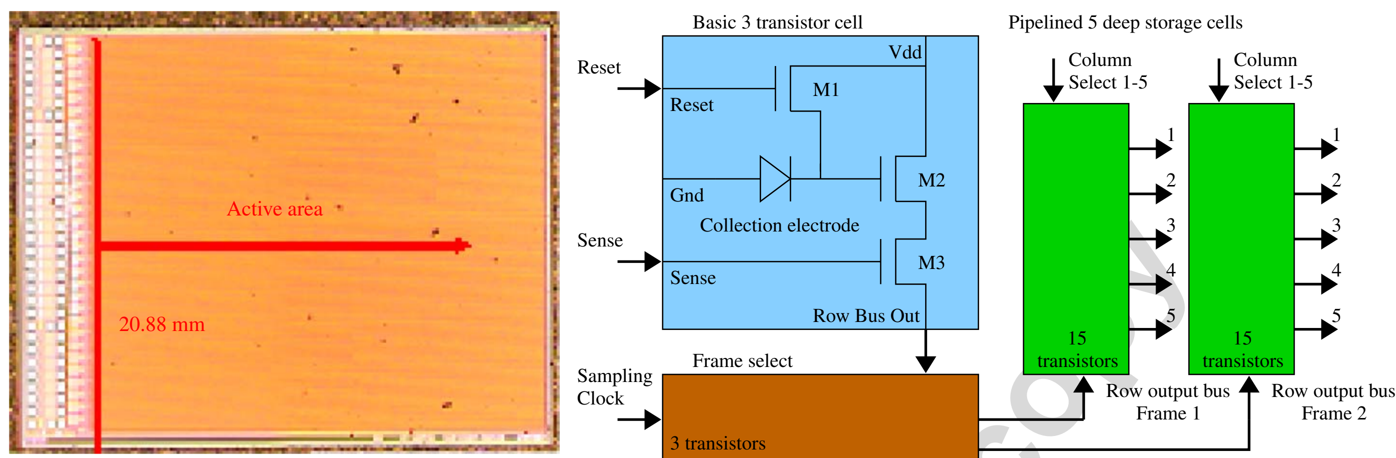

Fig. 2. Photograph of the CAP3 prototype with 928 × 128 pixels (left). For the sake of display convenience, the length has been rescaled. Pixel size is 22.5 μm × 22.5 μm and the active area covers 93% of the sensor size. The dead space is dominated by the scribe-line requirements, which could be reduced by precision dicing or active etching as part of the thinning procedure. A schematic of the pixel cell contents (right), with five sets of CDS pairs requires 36 transistors, thus a CAP3 sensor contains more than 4.3 M transistors.

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comparable to previous results [8]. After 200 kGy CAP1 retained full functionality and the effects at higher doses are not yet explored due to the time constraints of the irradiation facility. The results of CAP1 beam-test and radiation damage studies are presented in detail elsewhere [9].

2.2. The CAP3 design and plans for a pixel vertex detector

Based on the successful operation of CAP1 and CAP2 prototypes, design concept studies and plans for the next stages of R&D towards a full-size Pixel Vertex Detector (PVD) were undertaken and thus the third generation prototypes (CAP3), designed in the TSMC 0.25 μm process, was fabricated. The fabrication cost of the chip increases considerably at larger die sizes and is limited to about 21 mm in one direction by the maximum standard reticle size. Considering these constraints, a 3 by 21 mm CAP3 prototype was designed consisting of a 928 × 128 pixel array at 22.5 μm pitch, with a 5 deep sample pair pipeline in each pixel. While these could be treated as 10 independent samples, it is planned to use them, for operational convenience, as five CDS signals for direct use as differential reads. The $\sim 120 \times 10^3$ pixels of a single CAP3 chip (Fig. 2) correspond roughly to the number of the read-out channels of the present entire double-sided silicon-strip detector based SVD2. The critical point at making a practical read-out system is thus the ability to handle the enormous amount of data intrinsic to such a finely segmented detector.

As with the CAP2 prototype, the decoupling of the sampling frequency from the read-out frequency makes it possible to reduce the required data flow from CAP3, which would nevertheless at 10 kHz trigger rate still correspond to about 1.2×10^9 sample pairs per second. Data are transferred via 32 signal channels, with transfer rates of about 100 MHz to meet the latency requirements.

The task of the CAP3 front-end read-out system (PIXRO) is to subtract the two frames of analog data acquired in the pixel sensor arrays by CDS, pipeline the differentiated data into its memory, and send the data via an optical link to the back-end electronics. The base-line design is a high speed analog multiplexer, with the data digitalization on the back-end (FINESSE) side of the optical link. The PIXRO1 chip is based on the IBM 0.5 μm SiGe BiCMOS 5HP process[2] and can read out and subtract two full CAP3 frames in up to 100 μs, which satisfies the SuperBelle requirements. Low power consumption of the chip has been considered in the design. A schematic overview of a CAP3 based beam-test setup and a photograph of assembled laboratory test setup are shown in (Fig. 3).

3. Conclusions and future plans

After encouraging preliminary results of radiation hardness studies performed with CAP1 prototypes and the study of pipelined read out with CAP2 prototypes, CAP design looks promising for application in Belle. The physical dimensions of the CAP3 chip are large enough to be able to use it directly as a building block of the first generation pixel vertex detector (PVD). In the initial PVD upgrade, the plan is to keep the mechanical structure of the present Belle SVD2 system [10], which permits the possibility of an earlier installation without a redesign of the interaction region. CAP sensors would be used instead of the double-sided silicon-strip detectors (DSSD) in the first layer of the SVD only. The mechanical support for the

[2] MOSIS Integrated Circuit Fabrication Service, USC Information Sciences Institute, Marina del Rey, USA.

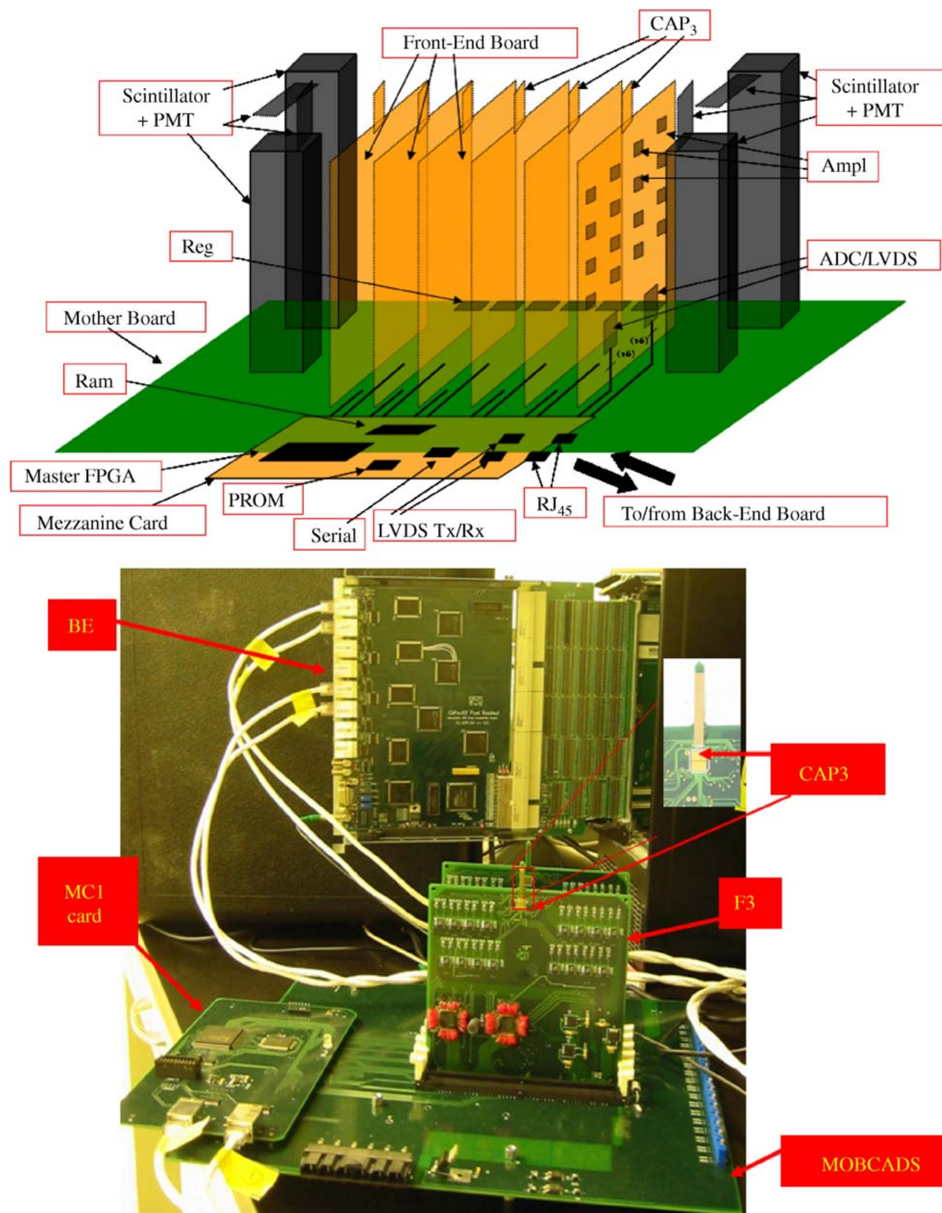

Fig. 3. Schematic view of a CAP3 based beam-test setup (top) and a photograph of assembled laboratory test setup (bottom). BE stands for the back-end and F3 for the front-end card which contains the CAP3 sensor and the ADC. Up to six F3 cards can be plugged into a MOBCADS, which provides routing between the F3 and the mezzanine card (MC1). MC1 contains the programmable gate array electronics, RAM memory for data storage and communicates with the BE board.

first layer DSSD has the form of six independent slightly overlapping planes (ladders), and each of these ladders can be fully populated using 36 CAP3 sensors per ladder. The operation of CAP3 sensor together with its read-out system is being extensively tested in the laboratory environment and a beam-test experiment is in preparation.

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